AF/2800

TRANSMITTAL OF APPEAL BRIEF

Docket No.
M4065.0477/P477

In re Application of: Kevin M. Devereaux

Application No.	Filing Date	Examiner	Group Art Unit
09/939,636-Conf. #4394	August 28, 2001	J. Nguyen	2815

Invention: METHOD AND APPARATUS FOR WAFER LEVEL TESTING OF SEMICONDUCTOR USING SACRIFICIAL ON DIE POWER AND GROUND METALIZATION

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed: July 7, 2003 .

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Dated: October 3, 2003

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Docket No.: M4065.0477/P477
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Kevin M. Devereaux

Application No.: 09/939,636 Confirmation No.: 4394

Filed: August 28, 2001 Art Unit: 2815

For: METHOD AND APPARATUS FOR WAFER LEVEL TESTING OF SEMICONDUCTOR USING SACRIFICIAL ON DIE POWER AND GROUND METALIZATION

Examiner: J. Nguyen

APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on July 7, 2003.

The fees required under § 1.17(f) and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief is transmitted in triplicate.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

I. Real Party In Interest
II Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments
V. Summary of Invention

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 19 claims pending in the application.

B. Current Status of Claims

1. Claims canceled: 12-24
2. Claims withdrawn from consideration but not canceled: N/A
3. Claims pending: 1-11 and 25-32
4. Claims allowed: None
5. Claims rejected: 1-11 and 25-32

C. Claims On Appeal

The claims on appeal are claims 1-11 and 25-32. A copy of the claims on appeal is attached as Appendix A.

IV. STATUS OF AMENDMENTS

Applicant filed an Amendment After Final Rejection on June 4, 2003. In an Advisory Action dated June 18, 2003, the Examiner indicated that Applicants' proposed amendments to claims 1, 9, 10 and 25 would be entered.

Accordingly, the claims enclosed herein as Appendix A incorporate the June 4, 2003 amendments to claims 1, 9, 10 and 25.

V. SUMMARY OF INVENTION

Figure 1a below shows a wafer 1 containing a plurality of fabricated dies 3. A sacrificial metal layer formed as a plurality of alternating sacrificial metal busses for a Vcc voltage (5) and a ground voltage Vss (7), are provided across the top surface of the wafer 1 and over the dies 3.

Figure 1b shows an expanded view of a Vcc 5 and Vss 7 bus which are provided over two adjacent dies 3. The bus metalization extends downwards through passivation layer openings in each die to respective on-die sacrificial Vcc pads 101 and Vss pads 201.

FIG. 1a

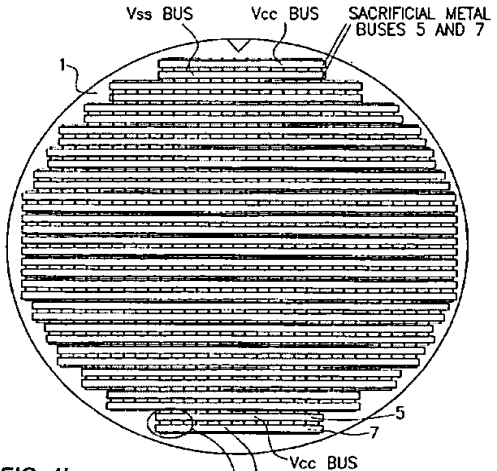
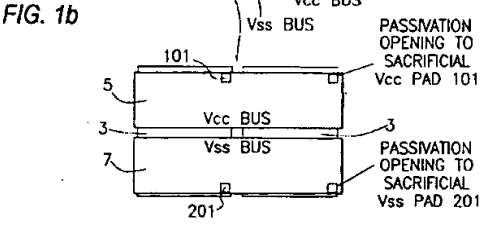


FIG. 1b

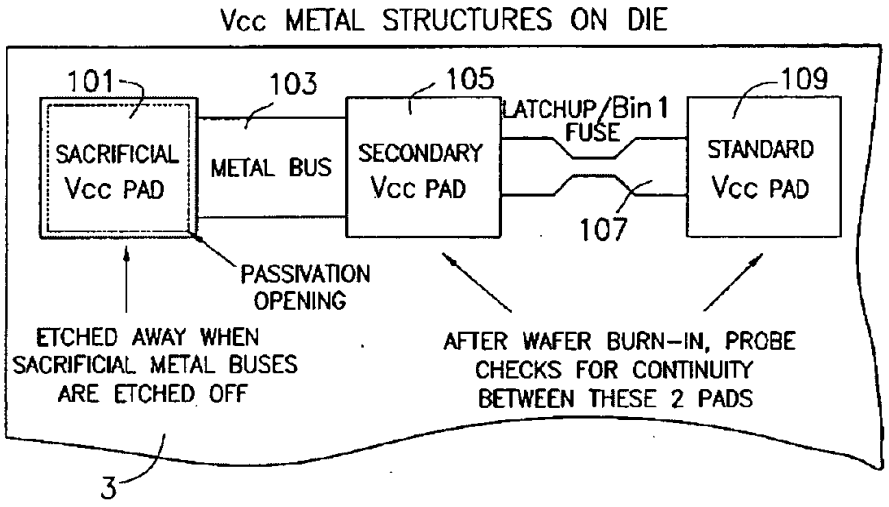


Referring to Figure 2 below, each die has a Vcc metalization path which includes three bonding pads, namely, a standard (normal) Vcc pad 109 for supplying operating voltage to internal circuitry within the die, a secondary Vcc pad 105 connected to the standard Vcc pad 109 through a fuse 107, and a sacrificial Vcc pad 101 connected to the secondary Vcc pad 105 through a metal bus 103. The pads 101, 105 and 109 are enlarged electrical connections which are used during various die testing procedures.

The standard Vcc pad 109 is a bond pad normally fabricated as part of the die 3 which is used to receive an external Vcc voltage and apply it to internal circuitry within a die 3. The secondary Vcc pad 105 is also fabricated on a die 3 and is connected to the standard Vcc pad 109 through a fuse 107 that is designed to blow in the event that a die 3 draws excessive current, for example, when a latch-up condition or other excessive current draw conditions which may occur during wafer level burn-in testing.

The sacrificial Vcc pad 101 supplies operating voltage to the die 3 during wafer level burn-in testing. This pad is etched away when the sacrificial metal layer, forming the Vcc 5 and Vss 7 busses, is removed from the wafer after testing. Sacrificial Vcc pad 101 is connected to secondary Vcc pad 105 through an on-die sacrificial metal Vcc bus 103 that is also partially removed when the Vcc 5 and Vss 7 busses are removed from the wafer. The sacrificial bus 103 protects the secondary Vcc pad 105 from being damaged when the sacrificial metal busses Vcc 5 and Vss 7 and the sacrificial Vcc pad 101 are etched away. The sacrificial metal bus 103 thus serves as a horizontal buffer for the secondary Vcc pad 105 when the sacrificial Vcc pad 101 is removed along with Vcc 5 and Vss 7 busses from the wafer.

FIG. 2



Referring to Fig. 4a below, a cross section of the uppermost layers of an exemplary die 3 with passivation and sacrificial Vcc metal layers provided for burn-in testing is shown. The passivation layer 301 covering the die 3 is etched to create a passivation opening 303 which exposes the sacrificial Vcc pad 101. A sacrificial Vcc metal layer 5 is provided atop the passivation layer 301 and is extended down to the sacrificial Vcc pad 101 through the passivation opening 303 on each die 3. A sacrificial metal bus 103 is formed between sacrificial Vcc pad 101 and secondary Vcc pad 105. After a first phase of testing, such as burn-in testing, is completed, sacrificial Vcc pad and possibly a portion of sacrificial metal bus 103 near the sacrificial Vcc pad is etched away such that secondary Vcc pad 105 is buffered from over-etching of sacrificial Vc pad 101. A latch-up fuse 107 is formed between the secondary Vcc pad 105 and standard Vcc pad 109. Standard Vcc pad 109 supplies operating voltage to circuitry within a respective die.

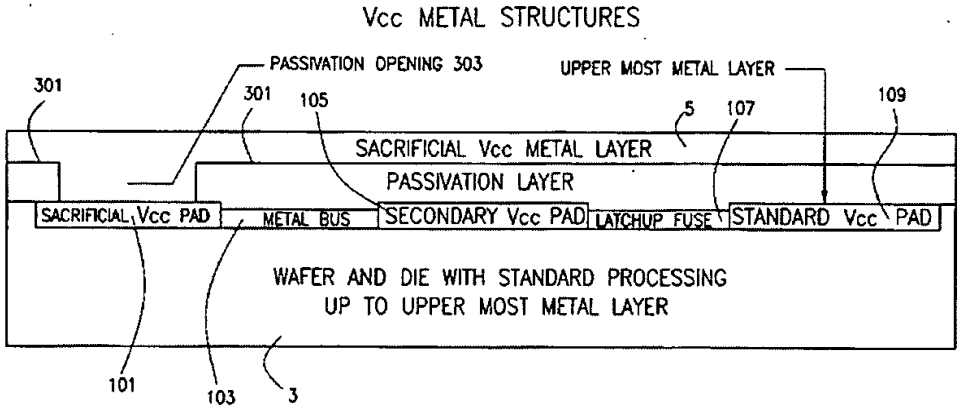


FIG. 4a

Referring to Figure 4b below, a cross section of the uppermost layers of the die 3 with passivation and sacrificial Vss metal structures provided for burn-in testing is shown. The passivation layer covering the die 301 is etched to create a passivation opening 305 which exposes the sacrificial Vss pad 201. A sacrificial Vss metal layer 7 is provided atop the passivation layer 301 and is extended down to the sacrificial Vss pad 201 through the Vss passivation opening 305. A metal bus 203 is formed between the sacrificial Vss pad 201 and a standard Vss pad 205.

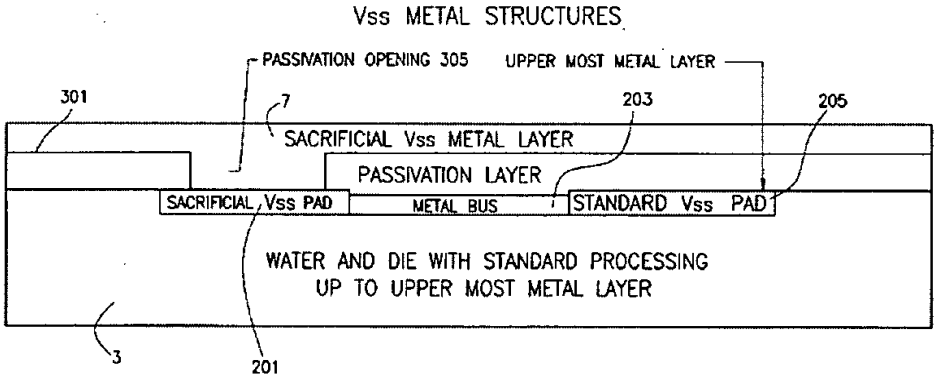


FIG. 4b

Thus, a unique wafer and die structure is provided for wafer level testing that includes fuses directly on the dies, and a sacrificial pad structure which protects non-sacrificial die pads (i.e., 101, 105, 205) from being etched when the sacrificial pads and sacrificial Vcc and Vss busses are removed.

VI. ISSUES

A. Whether claims 1-22 and 25-32 are properly rejected under 35 U.S.C. § 102(b) as being anticipated by Green, *et al.*

VII. GROUPING OF CLAIMS

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have been grouped as indicated below:

Group Claim(s)
I. Claims 1, 3, 5-7, 25, 27 and 29-31
II. Claim 2 and 26
III. Claim 4 and 28
IV. Claims 8 and 32
V. Claim 9-11

The claims of Group I stand or fall together. The claims of Group II stand or fall together. The claims of Group III stand or fall together. The claims of Group IV stand or fall together. The claims of Group V. stand or fall together. No claim stands or falls together with any claim of a different Group. In Section VIII below, Applicant has included arguments supporting the separate patentability of each claim group as required by M.P.E.P. § 1206.

VIII. ARGUMENTS

As Appellant discusses in detail below, the Final Rejection of claims 1-11 and claims 25-32 is devoid of any factual or legal premise that supports rejection.

A. The Anticipation Rejection of Claims 1, 3, 5-7, 25, 27 and 29-31 (Group I) Should be Reversed

Claims 1, 3, 5-7, 25, 27 and 29-31 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Green, *et al.* (hereinafter "Green").

Claim 1 is not anticipated by Green. Claim 1 recites a semiconductor wafer comprising, *inter alia*, "at least one first sacrificial conductive line ... a plurality of ... dies ... on said wafer, each die comprising ... a first terminal coupled to the circuitry within said die ... a second terminal ... a voltage interruption device provided between said first and second terminals for interrupting an electrical coupling between said first and second terminals ... and a first sacrificial terminal for receiving said first voltage from said first sacrificial conductive line ...." Appellant respectfully submits that Green fails to disclose, teach or suggest such a structural combination.

Green discloses a semiconductor wafer testing fixture that facilitates burn-in testing of multiple wafers, wherein individual wafers have an array of individual die with their own test circuitry. (Green, COL. 2, lines 43-45) The Green wafer 10 includes an array of integrated circuit dies 12 beneath sacrificial Vcc and Vss busses 24 and 28, where each die 12 comprises a series of bonding pads 32 and 34 which extend to integrated circuitry formed within each of the dies 12 (Green, COL. 4, lines 28-32) (Figure 3 of Green is reproduced below).

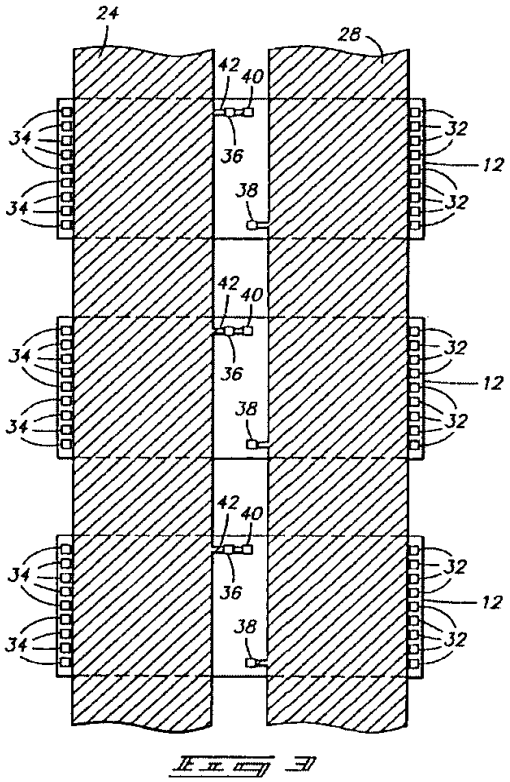
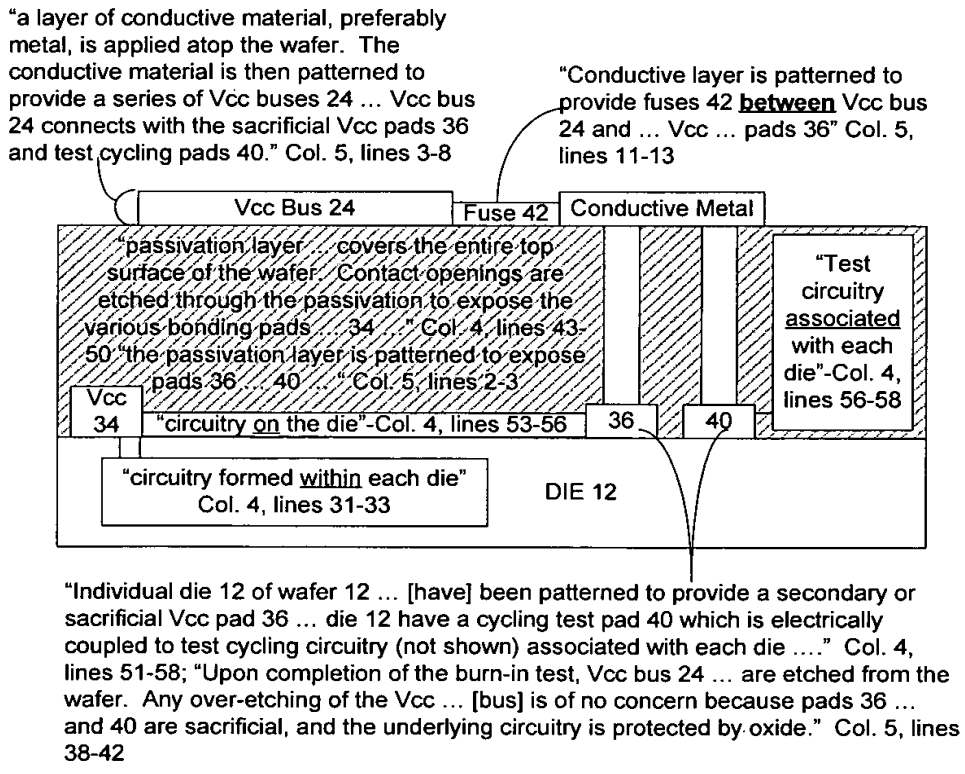


Fig. 3

Figure 3 discloses dies 12 which have been formed with sacrificial Vcc pad 36. Green at COL. 4, lines 51-56 states that each sacrificial Vcc pad 36 is connected by circuitry on each die to a corresponding permanent Vcc pad 32. Additionally, each die 12 has a cycling test pad 40 which is electrically coupled to test cycling circuitry (not shown) associated with each die 12. (Green, COL. 4, lines 56-58). Vcc bus 24 connects with the sacrificial Vcc pads 36 and test cycling pads 40. (Green, COL. 5, lines 7-10). A conductive layer is initially formed above a passivation layer (not shown in the drawings) deposited on the entire wafer 10, including over pads 32, 36 and 40, and openings are etched to pads 36, 40. (Green, COL. 4, lines 43-50; COL 5, lines 2-3). Vcc bus 24 and fuses 42 are formed above the passivation layer connected to pads 36, 40 by patterning the conductive layer. (Green, COL. 5, lines 1-15). A cross sectional view of Green is provided below which illustrates Green's bus, fuse, metalization and die structure – the view shown below has been created by Applicant based upon both FIG. 3 of Green and the above referenced excerpts of COL. 4 lines 28 through COL. 5, line 1-15, 37-41.



Green, Cross Sectional View

It should be understood that the above Green Cross Sectional View, as well as other Green figures provided by Appellant, are based on Appellant's best understanding of Green in view of both FIG. 3 and the cited portions of the specification. However, Green does not clearly explain a number of aspects of the FIG. 3 structures including, for example, the precise vertical position of sacrificial Vcc pads 36 and 40 and exactly how those pads connect with other structures. All that is known about vertical positioning of Vcc pads 36 and 40 is that they are somewhere within the passivation layer as openings are described as being etched into the passivation layer to expose sacrificial Vcc pads 36, 40 in order to connect with the conductive layer above the passivation layer.

The Final Rejection on page 2, first paragraph states that the first terminal recited in claim 1 corresponds to Green's Vcc pad 34, the second terminal recited in claim 1 corresponds to Green's sacrificial Vcc pad 36 and the voltage interruption device for interrupting an electrical coupling between the first and second terminal recited in claim 1 corresponds to Green's fuse 42.

Claim 1 recites, *inter alia*, "a voltage interruption device provided between said first and second terminals for interrupting an electrical coupling between said first and second terminals ...." Green's fuse 42 does not meet this limitation since it is not located between Vcc pad 34 and sacrificial Vcc pad 36. Rather, Green's fuse 42 is actually part of the conductive layer on the top of the passivation layer that is "patterned to provide fuses 42 between Vcc bus 24 and individual Vcc sacrificial pads 36...." Green, Col. 5, lines 11-13 (See the cross-sectional depiction of Green on the preceding page). The Examiner appears to have been misled by Green's Fig. 3 which is a top view and does not show portions of the die and wafer including the passivation layer formed above Vcc pads 34, 36 and 40 as well as underlying electrical connection between Vcc pad 34 and sacrificial Vcc pad 36.

Also, claim 1 recites, *inter alia*, "a first terminal coupled to circuitry within said die for supplying [a] ... first voltage to ... circuitry [within a die]... a second terminal for supplying said first voltage to said first terminal ... a voltage interruption device provided between said first and second terminals ... and a first *sacrificial* terminal for receiving said

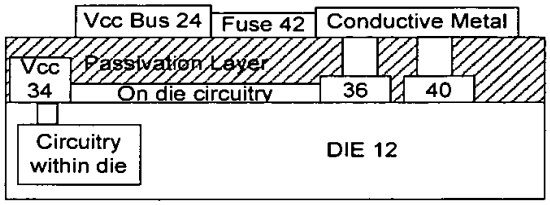
first voltage from said first sacrificial conductive line and supplying said first voltage to said second terminal." (emphasis added) Green discloses that Vcc pad 36 (which the Examiner equates to Applicant's "second terminal") and test cycling pad 40 are sacrificial and fuses 42 are sacrificial (Green, COL. 5, lines 38-41), unlike claim 1 where the "second terminal" is defined as the voltage supply terminal and is not sacrificial.

Accordingly, for at least the foregoing reasons, claim 1 is allowable over Green. Claims 2-8 depend from claim 1, thus are allowable along with claim 1 and for other reasons.

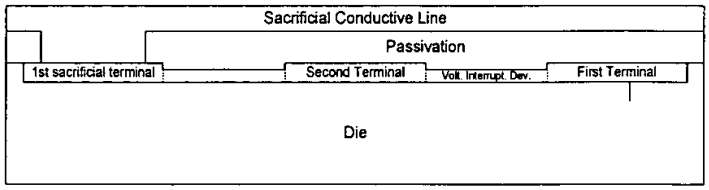
Claim 25 is not anticipated by Green. Claim 25 recites, *inter alia*, "[a] first sacrificial conductive line for supplying a first voltage to a plurality of dies ... on ... [a] wafer ... each die comprising: a first terminal coupled to ... circuitry within said die for supplying [a] ... first voltage to said circuitry ... a voltage interruption device coupled to said first terminal ... a second terminal coupled to said voltage interruption device, said interruption device for interrupting an electrical coupling between said first and second terminals ... and a first sacrificial terminal electrically coupled to said second terminal for receiving said first voltage from said first sacrificial conductive line" The Final rejection states that Green discloses in figure 3 all the structure set forth in claim 25 on page 5 of the Final Rejection.

As shown below, Green discloses fuse 42 between Vcc bus 24 and sacrificial Vcc pad 36. In contrast to Green, the Exemplary Claim 25 Figure (an annotated version of Fig. 4a depicted below) shows the claim 25 "voltage interruption device coupled to said first terminal [and] ... a second terminal coupled to said voltage interruption device ...." Moreover, since fuse 42 in Green is not between the permanent Vcc 34 pad and either pad 36 or 40, fuse 42 does not interrupt "electrical coupling *between* said first and second terminals ..." as further recited by claim 25. (emphasis added) Consequently, Green does not disclose the same coupling between the voltage interruption device and the first and second terminal of claim 25, as these terminals are defined in claim 25; thus, claim 25 is

allowable over Green. Claims 26-32 depend directly or indirectly from claim 25, thus are allowable along with claim 25 and for other reasons.



Green



Exemplary Claim 25 Figure

Accordingly, Appellant respectfully submits that the rejection of claims 1, 3, 5-7, 25, 27 and 29-31 under 35 U.S.C. § 102(b) should be reversed.

B. The Anticipation Rejection of Claims 2 and 26 (Group II) Should be Reversed

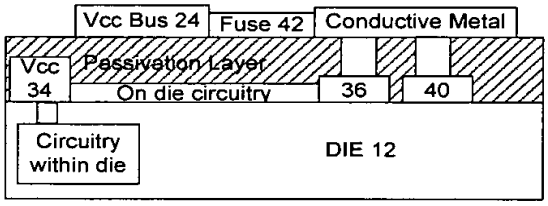
Claims 2 and 26 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Green.

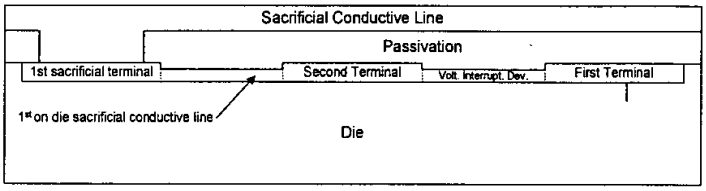
Claim 2 is not anticipated by Green. Claim 2 recites "the wafer of claim 1 wherein each die further comprises a first on-die sacrificial conductive line provided between the first sacrificial terminal and second terminal." The Final Rejection states on page 3 that Green discloses in figures 2 and 3 that each die 12 further comprises a first on-die sacrificial conductive line provided between the first sacrificial terminal 40 and second terminal 36, as recited in claim 2.

Initially, it is noted that claim 2 depends from claim 1 and is allowable for at least the reasons set forth above with respect to claim 1.

As shown below, Green only discloses "a layer of conductive material ... applied atop the wafer ... patterned to provide a series of Vcc buses 24" [COL. 5, lines 3-6] ... [and] fuses 42 between Vcc bus 24 and individual Vcc sacrificial pads 36 ...." [COL. 5,

lines 5-6; 11-12], not "on-die" as recited in claim 2. (Green, COL. 4, lines 43-50; COL. 5, lines 1-15) Also, the only connection disclosed between pads 34, 36 and 40 is on-die circuitry which connects Vcc pad 34 and secondary Vcc pad 36, which is not described as sacrificial. (Green, COL. 4, lines 53-55) Consequently, Green does not discloses "a first *on-die sacrificial* conductive line provided *between* the first sacrificial terminal and second terminal" as recited in claim 2.





Green Exemplary Figure For Claim 2

Claim 26 is not anticipated by Green. Claim 26 recites "the wafer of claim 25 wherein each die further comprises a first on-die sacrificial conductive line provided between the first sacrificial terminal and second terminal." The Final Rejection states on page 5 that figure 3 in Green discloses all claim elements of claim 26.

Claim 26 depends from claim 25 and is allowable for at least the reasons set forth above with respect to claim 25.

Green also does not disclose "a second terminal coupled to [a] ... voltage interruption device for interrupting an electrical coupling between said first and second terminals" as in claim 25, much less the "... on-die sacrificial conductive line provided between the first sacrificial terminal and second terminal" as recited in dependent claim 26. Accordingly, Green fails to disclose, teach or suggest the subject matter of claim 26.

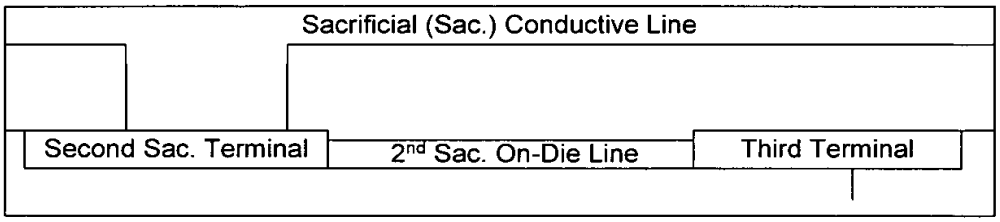
Appellant respectfully submits that the rejection of claims 2 and 26 under 35 U.S.C. § 102(b) should be reversed.

C. The Anticipation Rejection of Claims 4 and 28 (Group III) Should be Reversed

Claims 4 and 28 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Green.

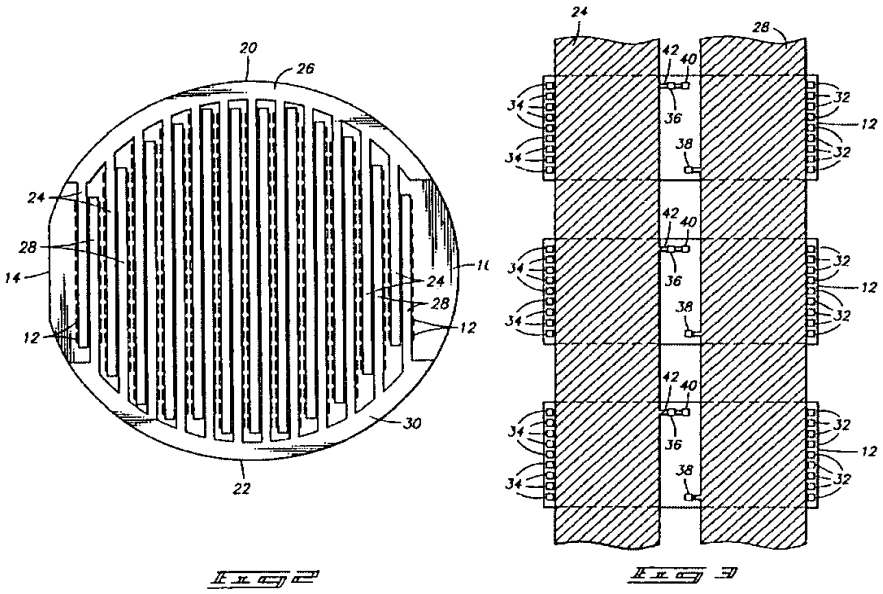
Claim 4 is not anticipated by Green.

Claim 4 recites "the wafer of claim 3, wherein each die further comprises a second on-die sacrificial conductive line provided between the second sacrificial terminal and third terminal." One embodiment of the claim 4 structure is disclosed in the Vss structure of Fig. 4b.



Exemplary Claim 4 Figure

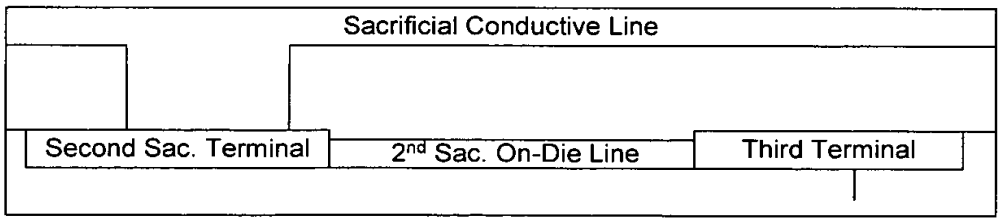
The Final Rejection at page 4 states that Green discloses in figures 2 and 3 (shown below) each die 12 further comprising a second on-die sacrificial conductive line provided between the second sacrificial terminal 38 and third terminal 32.



Initially, it is noted that claim 4 depends from claims 3 and 1 and is allowable for at least the reasons set forth above with respect to claims 3 and 1.

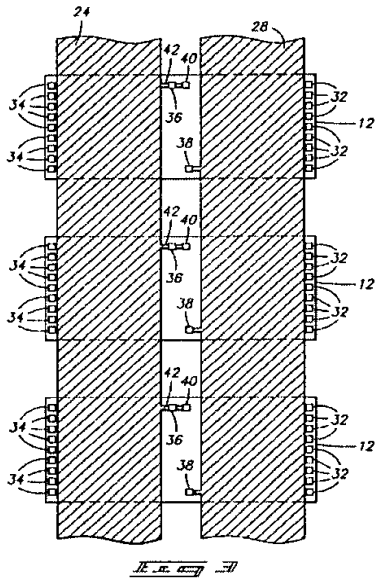
Green at COL. 4, lines 54-55 states that sacrificial Vss pad 38 is connected by circuitry on the die to the permanent Vss pad 32. Nowhere does Green disclose, *inter alia*, an "on-die sacrificial conductive line provided between the second sacrificial terminal and third terminal ...." There is no mention in Green that the circuitry on the die connecting sacrificial Vss pad 38 to Vcc pad 32 is sacrificial. Accordingly, Green does not disclose, teach or suggest, *inter alia*, a "second on-die sacrificial conductive line provided between the second sacrificial terminal and third terminal".

Claim 28 is not anticipated by Green. Claim 28 recites, *inter alia*, "each die further comprises a second on-die sacrificial conductive line provided between the second sacrificial terminal and third terminal."



Exemplary Claim 28 Figure

The Final Rejection at page 5 states that Green discloses in figure 3 all of the structure set forth in claim 28.



It is noted that claim 28 depends from claims 27 and 25 and is allowable for at least the reasons set forth above with respect to claim 27 and 25.

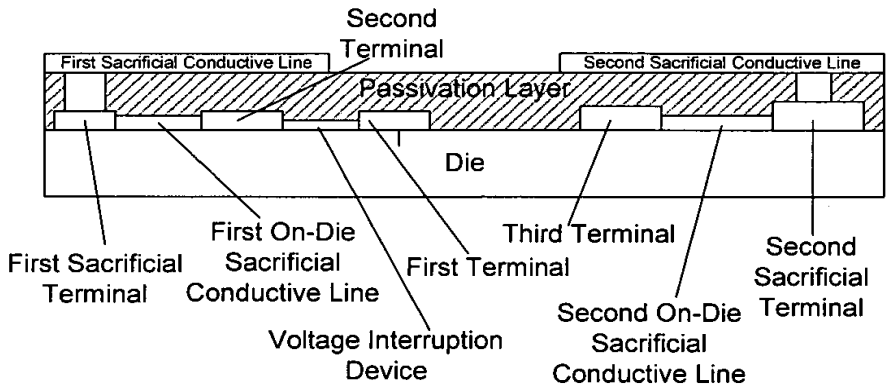
As shown above, Green does not disclose a sacrificial conductive line provided between the second sacrificial terminal and third terminal. (Green at COL. 4, lines 54-55) There is no disclosure whatsoever in FIG. 3 of any conductive line, much less a sacrificial conductive line, between pad 38 and pad 32. Green, FIG. 3 only discloses a part of sacrificial Vss bus 28 coupled with pad 38. Accordingly, claim 28 is allowable over Green.

Appellant respectfully submits that the rejection of claims 4 and 28 under 35 U.S.C. § 102(b) should be reversed.

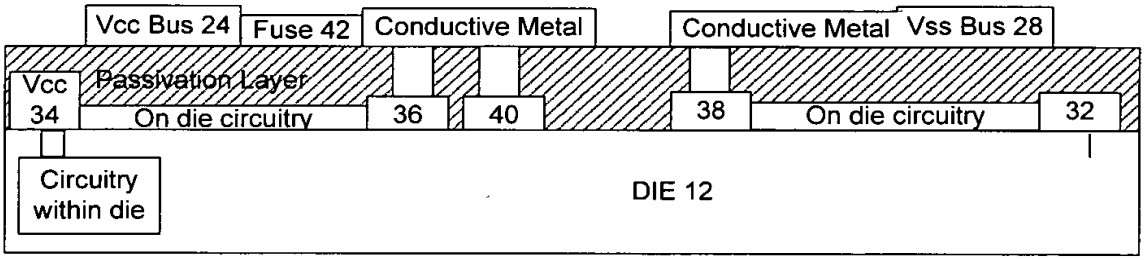
D. The Anticipation Rejection of Claims 8 and 32 (Group IV) Should be Reversed

Claims 8 and 32 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Green.

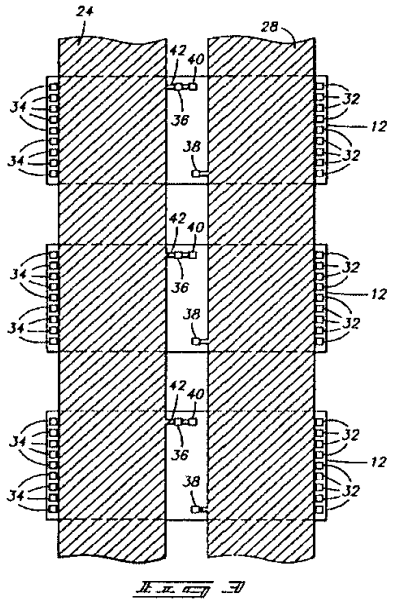
Claim 8 is not anticipated by Green As shown below, claim 8 recites, *inter alia*, "a first on-die sacrificial conductive line provided between the first sacrificial terminal and second terminal; and a second on-die sacrificial conductive line provided between the third terminal and the second sacrificial terminal." In the preferred embodiment of Applicant's invention, this would correspond to a structure formed of a combination of Figs. 4a and 4b as follows:



Exemplary Claim 8 Figure



Representation of Green Based on FIG. 3 and Specification of Green



Green Figure 3

The Final Rejection on pages 3-4 states with regard to claim 8 that Green discloses in figures 2 and 3 a first on-die sacrificial conductive line provided between the first sacrificial terminal; and a second on die sacrificial conductive line provided between the third terminal and second sacrificial terminal.

Initially, it is noted that claim 8 depends from claims 7, 3 and 1 and is allowable for at least the reasons set forth above with respect to claims 7, 3 and 1.

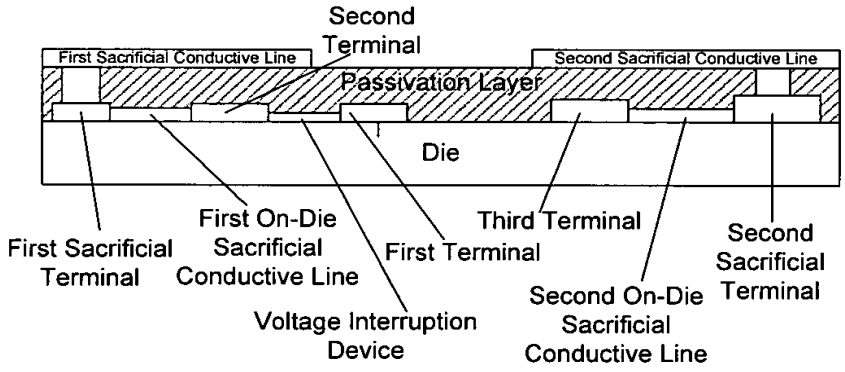
Green does not disclose a "a first on-die sacrificial conductive line provided between the first sacrificial terminal and second terminal; and a second on-die sacrificial conductive line provided between the third terminal and the second sacrificial terminal." Green states at COL. 4, lines 52-58 that "Sacrificial Vcc pad 36 and sacrificial Vss pad 38 are connected by circuitry on the die to the permanent Vcc pad and Vss pad of peripheral pads 32, 34." There is no disclosure in Green that "the circuitry on the die" coupling Vcc pads 36 and 34 as well as Vss pads 38 and 32 are sacrificial. Green at COL. 5, lines 37-42 states "... over-etching of the Vcc and Vss busses is of no concern because pads 36, 38 and 40 are sacrificial, and the underlying circuitry is protected by oxide." Thus, there is no teaching

or suggestion of a "second on-die sacrificial conductive line provided between the third terminal and the second sacrificial terminal" as in claim 8.

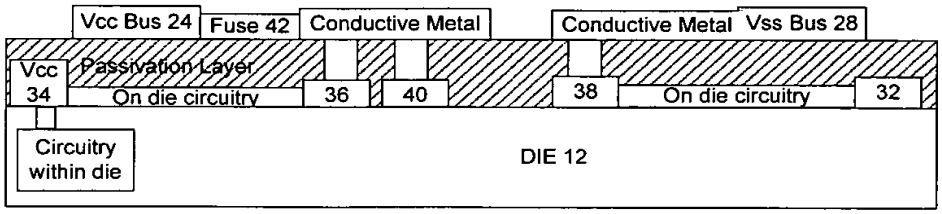
Claim 32 is not anticipated by Green. Claim 32 recites, *inter alia*, "a first on-die sacrificial conductive line provided between the first sacrificial and second terminal; and a second on-die sacrificial conductive line provided between the third terminal and the second sacrificial terminal as recited in claim 32. The Final Rejection on page 5 states that figure 3 of Green discloses the subject matter of claim 32.

Initially, it is noted that claim 32 depends from claims 31, 27 and 25 and is allowable for at least the reasons set forth above with respect to claims 31, 27 and 25.

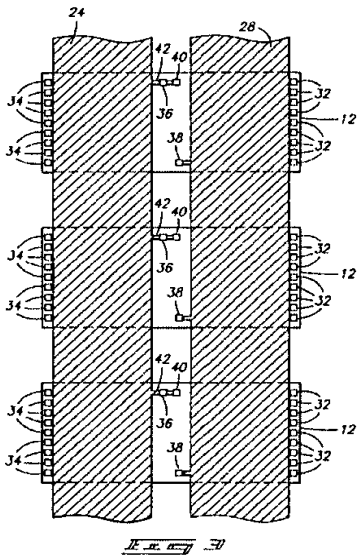
As shown below, Green at COL. 4, lines 54-55 states that sacrificial Vcc pad 36 and sacrificial Vss pad 38 are connected by circuitry on the die to the permanent Vcc and Vss pads 34, 32. Green at COL. 5, lines 41-42 states that the underlying circuitry associated with sacrificial Vcc pad 36 and Sacrificial Vss pad 38 is protected by oxide from over etching at the completion of burn-in testing.



Exemplary Claim 32 Figure



Representation of Green Based on FIG. 3 and Specification of Green



Green Figure 3

Accordingly, Green does not disclose, teach or suggest, *inter alia*, "a first on-die sacrificial conductive line provided between the first sacrificial and second terminal; and a second on-die sacrificial conductive line provided between the third terminal and the second sacrificial terminal" as recited in claim 32.

For at least the foregoing reasons, claims 8 and 32 are allowable over Green. Accordingly, Appellant respectfully submits that the rejections of claims 2 and 32 under 35 U.S.C. § 102(b) should be reversed.

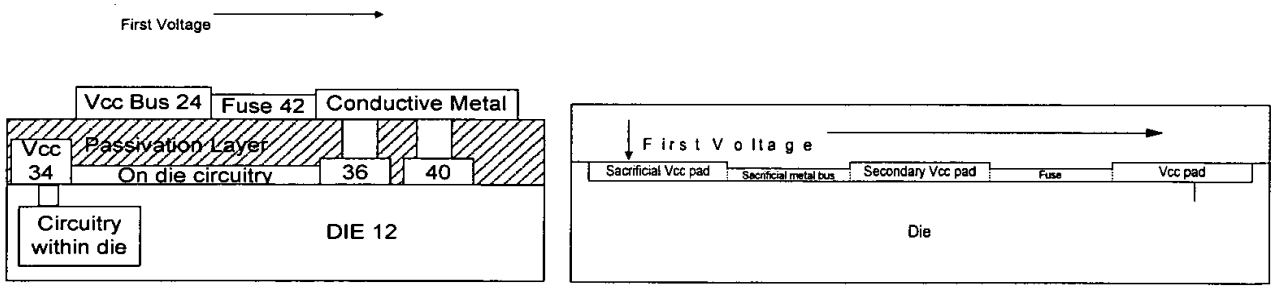
E. The Anticipation Rejection of Claims 9-11 (Group V) Should be Reversed

Claims 9-11 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Green.

Claim 9 is not anticipated by Green. Claim 9 recites, *inter alia*, "a semiconductor die comprising ... a Vcc bonding pad coupled to the circuitry within said die for supplying a first voltage to said circuitry ... a secondary Vcc bonding pad a fuse ... between the Vcc

bonding pad and the secondary Vcc bonding pad, said secondary Vcc bonding pad supplying said first voltage through said fuse to the Vcc bonding pad, said fuse adapted for interrupting electrical coupling between the secondary Vcc bonding pad and said Vcc bonding pads ... a sacrificial Vcc bonding pad for receiving said first voltage ... and a sacrificial metal bus interconnected between the sacrificial Vcc bonding pad and secondary Vcc bonding pad for receiving said first voltage from the sacrificial Vcc bonding pad and supplying said first voltage to the secondary Vcc bonding pad."

The Final Rejection on page 4 states Green discloses "on figure 3 a semiconductor die 12 comprising a standard Vcc bonding pad 34 coupled to the circuitry within said die 12 for supplying a first voltage to said circuitry; a secondary Vcc bonding pad 36; a fuse 42 interconnected between the standard Vcc bonding pad supplying said first voltage through said fuse 42 to the Vcc bonding pad ... a sacrificial Vcc bonding pad 40 ... a sacrificial metal (readable on figure 3) interconnected between the sacrificial Vcc pad and secondary Vcc bonding pad for receiving said first voltage from the sacrificial Vcc bonding pad and supplying said first voltage to the secondary Vcc bonding pad."



Green Exemplary Claim 9 Figure

Claim 9 recites, *inter alia*, "a secondary Vcc bonding pad ... supplying said first voltage through said fuse to the Vcc bonding pad. As shown above, Green's secondary Vcc bonding pad 36 does not supply said first voltage through said fuse to the Vcc bonding pad 34.

Claim 9 further recites, *inter alia*, "a secondary Vcc bonding pad ... a sacrificial Vcc bonding pad ... a sacrificial metal bus interconnected between the sacrificial Vcc bonding pad and secondary Vcc bonding pad for receiving said first voltage from the sacrificial Vcc bonding pad and supplying said first voltage to the secondary Vcc bonding pad."

As shown above, Green's sacrificial test cycling pad 40 does not supply "said first voltage to the secondary Vcc bonding pad [36]". To the contrary, conductive metal formed as a part of the Vcc bus 24 supplies voltage first to Green's secondary Vcc pad 36 and then to the test cycling pad 40. (Green, COL. 5, lines 3-10)

Claim 9 further recites, *inter alia*, "sacrificial metal bus interconnected between the sacrificial Vcc bonding pad and secondary Vcc bonding pads ..." where "a fuse [is] interconnected between ... Vcc bonding pad and the secondary bonding pad ...." Green does not disclose such a combination. First, Green's test cycling pad 40 cannot be the secondary bonding pad of claim 9. Green does not disclose a fuse 42 coupled between Vcc pad 34 and secondary Vcc pad 36. (Green, COL. 4, lines 44-45; 51-58; COL. 5, lines 1-15; lines 35-42) Accordingly Green does not disclose a combination of "a sacrificial metal bus interconnected between the sacrificial Vcc bonding pad and secondary Vcc bonding pad ..." as recited in claim 9.

For at least the foregoing reasons, claim 9 is allowable over Green. Claims 10-11 depend from claim 9, thus are also allowable along with claim 9. Appellant respectfully submits that the rejection of claims 9-11 under 35 U.S.C. § 102(b) should be reversed.

IX. CONCLUSION

For the reasons given above, it is respectfully submitted that the final rejection of claims 1-11 and 25-32 is improper. Accordingly, Appellant requests reversal of all rejections by this honorable Board.

X. CLAIMS INVOLVED IN THE APPEAL

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A include the amendments filed by Applicant on June 4, 2003.

Dated: October 3, 2003

Respectfully submitted,

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/939,636

1. A semiconductor wafer comprising:

at least one first sacrificial conductive line for supplying a first voltage to a plurality of dies fabricated on said wafer;

a plurality of integrated circuit dies fabricated on said wafer, each die comprising:

a first terminal coupled to the circuitry within said die for supplying said first voltage to said circuitry;

a second terminal for supplying said first voltage to said first terminal;

a voltage interruption device provided between said first and second terminals for interrupting an electrical coupling between said first and second terminals; and

a first sacrificial terminal for receiving said first voltage from said first sacrificial conductive line and supplying said first voltage to said second terminal.

2. The wafer of claim 1 wherein each die further comprises a first on-die sacrificial conductive line provided between the first sacrificial terminal and second terminal.

3. The wafer of claim 1 further comprising:

at least one second sacrificial conductive line for supplying a second voltage to said plurality of dies;

each die further comprising:

a third terminal coupled to the circuitry within said die for supplying a second voltage to said circuitry; and

a second sacrificial terminal for receiving said second voltage from said sacrificial second conductive line and supplying said second voltage to said third terminal.

4. The wafer of claim 3 wherein each die further comprises a second on-die sacrificial conductive line provided between the second sacrificial terminal and third terminal.

5. The wafer of claim 1 wherein the voltage interruption device is a fuse.

6. The wafer of claim 5 wherein said fuse is blown when said die draws current in excess of a predetermined value.

7. The wafer of claim 3 wherein each die further comprises:

a passivation layer having respective openings to the first and second sacrificial terminals, said first and second sacrificial terminals respectively connecting with said first and second sacrificial conductive lines through said openings.

8. The wafer of claim 7 further comprising:

a first on-die sacrificial conductive line provided between the first sacrificial terminal and second terminal; and

a second on-die sacrificial conductive line provided between the third terminal and the second sacrificial terminal.

9. A semiconductor die comprising:

a Vcc bonding pad coupled to the circuitry within said die for supplying a first voltage to said circuitry;

a secondary Vcc bonding pad;

a fuse interconnected between the Vcc bonding pad and the secondary Vcc bonding pad, said secondary Vcc bonding pad supplying said first voltage through said fuse to the Vcc bonding pad, said fuse adapted for interrupting electrical coupling between the

secondary Vcc bonding pad and said Vcc bonding pads when the die draws current in excess of said fuse breakdown current;

a sacrificial Vcc bonding pad for receiving said first voltage; and

a sacrificial metal bus interconnected between the sacrificial Vcc bonding pad and secondary Vcc bonding pad for receiving said first voltage from the sacrificial Vcc bonding pad and supplying said first voltage to the secondary Vcc bonding pad.

10. The semiconductor wafer of claim 9 further comprising:

a Vss bonding pad coupled to the circuitry within said die for supplying a second voltage to said circuitry;

a sacrificial Vss bonding pad for supplying the second voltage to the Vss bonding pad; and

a sacrificial metal bus which connects the sacrificial Vss bonding pad and the Vss bonding pad.

11. The semiconductor die of claim 10 further comprising:

a passivation layer which is provided with respective openings to the sacrificial Vcc and Vss bonding pads; and

Vcc and Vss sacrificial conductive busses formed over said passivation layer, said Vcc sacrificial conductive bus passing through an opening in said passivation layer to connect with said Vcc sacrificial bonding pad and said Vss sacrificial conductive bus passing through an opening in said passivation layer to connect with said Vss sacrificial bonding pad.

12 – 24 (Cancelled in response to restriction requirement)

25. A semiconductor wafer comprising:

at least one first sacrificial conductive line for supplying a first voltage to a plurality of dies fabricated on said wafer;

a plurality of integrated circuit dies fabricated on said wafer, each die comprising:

a first terminal coupled to the circuitry within said die for supplying said first voltage to said circuitry;

a voltage interruption device coupled to said first terminal;

a second terminal coupled to said voltage interruption device, said interruption device for interrupting an electrical coupling between said first and second terminals; and

a first sacrificial terminal electrically coupled to said second terminal for receiving said first voltage from said first sacrificial conductive line and supplying said first voltage to said second terminal.

26. The wafer of claim 25 wherein each die further comprises a first on-die sacrificial conductive line provided between the first sacrificial terminal and second terminal.

27. The wafer of claim 25 further comprising:

at least one second sacrificial conductive line for supplying a second voltage to said plurality of dies;

each die further comprising:

a third terminal coupled to the circuitry within said die for supplying a second voltage to said circuitry; and

a second sacrificial terminal for receiving said second voltage from said sacrificial second conductive line and supplying said second voltage to said third terminal.

28. The wafer of claim 27 wherein each die further comprises a second on-die sacrificial conductive line provided between the second sacrificial terminal and third terminal.

29. The wafer of claim 25 wherein the voltage interruption device is a fuse.

30. The wafer of claim 29 wherein said fuse is blown when a said die draws current in excess of a predetermined value.

31. The wafer of claim 27 wherein each die further comprises:

a passivation layer having respective openings to the first and second sacrificial terminals, said first and second sacrificial terminals respectively connecting with said first and second sacrificial conductive lines through said openings.

32. The wafer of claim 31 further comprising:

a first on-die sacrificial conductive line provided between the first sacrificial terminal and second terminal; and

a second on-die sacrificial conductive line provided between the third terminal and the second sacrificial terminal.